JOHN PETER STEVENSON

10 CANEPA CT. REDWOOD CITY, CA 94062 (650) 906-9549 | etep.nosnevets@gmail.com

EDUCATION

FXPFRIFNCF

Stanford University 2008 - 2014 Ph.D. Electrical Engineering

Thesis: Fine-Grain In-Memory Deduplication for Large-Scale Workloads

Stanford University 2000 - 2002 M.S. Electrical Engineering

Focus on circuit design and semiconductor physics

U.S. Naval Academy 1996 - 2000 B.S. Control Systems Engineering

Graduated 1st in academic standing

HONORS & AWARDS

Best Paper

Sparse Matrix-Vector Multiply on the HI-CAMP Architecture, International Conference on Supercomputing

Best Startup Project 2011 Stanford MS&E-273: Punch Mobile

David Cheriton Fellow 2008 - 2014 Stanford Graduate Fellowship

SOE Fellow 2000 - 2002

Stanford School of Engineering Fellowship

Ward Prize

2000 Best undergraduate research for a multiaperture camera array

PKP NHS Fellow

Phi Kappa Phi National Honor Society Graduate Study Fellowship

Rhodes Finalist	1999

Eagle Scout

Pixie Labs & New Relic Founding & Principal Engineer | San Francisco, CA

2020 - Present

Led development of eBPF performance profiler. Developed continuous performance regression testing framework. Implemented record & replay test & development feature.

Citadel Securities

Quantitative HW/SW Developer | Chicago, IL

Hardware software co-design for low latency trading. Implemented machine learning algorithms in FPGA. Wrote hardware emulator for model training.

Intel

2012

2000

1996

2014 - 2016

2016 - 2020

Silicon Architect | Santa Clara, CA

Developed next generation memory technology as a member of the HICAMP team acquired in 2014. Wrote CPU cache performance simulator to validate key aspects of the technology. Contributed micro-architectural optimizations. Developed strong low latency hardware hash functions.

HICAMP Systems

Member of Technical Staff | Menlo Park, CA

Member of seven person engineering team, firm and technology acquired by Intel in 2014. Contributed to FPGA implementation of next generation CPU memory controller.

U.S. Naval Academy

2006 - 2008

2009 - 2014

Electrical Engineering Faculty | Annapolis, MD

Taught undergraduate engineering major and core curriculum classes for 4 semesters, as an officer faculty member. Topics included circuit analysis, logic design, and wireless.

Lawrence Livermore National Laboratory Photonics Group Intern | Livermore, CA

Studied wavelength shifts for photonic logic gate laters.

USS Los Angeles (SSN-688)

2003 - 2006

2007

Officer | Honolulu, HI

As Officer of the Deck, responsible for all operations submerged, surfaced, and in port, in lieu of the ship's Captain. As Engineering Officer of the Watch, responsible for all nuclear power plant operations, in lieu of the ship's Engineer. Supervised a shipboard division.

Honda Research

Computer Vision Intern | Mountain View, CA

Depth recovery algorithms for non-stereoscopic images.

Tensilica

Design Verification Intern | Sunnyvale, CA

2001

2002

Wrote scripts to drive verification for customizable RTL code.

SITM

SI-TM: Reducing Transactional Memory Abort Rates through Snapshot Isolation

H. Litz, D. Cheriton, A. Firoozshahian, O. Azizi, J.P. Stevenson, ASPLOS 2014

SpMV on HICAMP

Sparse Matrix-Vector Multiply on the HI-CAMP Architecture

J.P. Stevenson, A. Firoozshahian, A. Solomatnikov, M. Horowitz, and D. Cheriton, ICS 2012

Winner of Best Paper Award at International Conference on Supercomputing, 2012

HICAMP

HICAMP: Architectural Support for Efficient Concurrency-Safe Shared Structured Data Access

D. Cheriton, A. Firoozshahian, A. Solomatnikov, J.P. Stevenson, and O. Azizi, ASP-LOS 2012

CPU db

CPU db: Recording Microprocessor History

A. Danowitz, K. Kelley, J. Mao, J.P. Stevenson, and M. Horowitz, CACM 2012

IR for ChipGen

Intermediate Representations for Controllers in Chip Generators

K. Kelley, M. Wachs, A. Danowitz, J.P. Stevenson, S. Richardson, M. Horowitz, DATE 2011

CPU Co-Optimization

An Integrated Framework for Co-Optimization of Architecture and Circuits

O. Azizi, A. Mahesri, J.P. Stevenson, N. Zhou, S.J. Patel, and M. Horowitz, DATE 2010

PATENTS

2014 Customized Memory Deduplication

2010

C. Egbert, A. Firoozshahian, M. Maddury, J.P. Stevenson, H. Neefs, O. Azizi

Hardware-Assisted Paging Mechanisms 2018

A. Firoozshahian, O. Azizi, C. Egbert, D. Hansen, A. Kleen, M. Maddury, M. Madhav, A. Solomatnikov, J.P. Stevenson

Searchable Hot Content Cache

Omid Azizi, A. Solomatnikov, A. Firoozshahian, J.P. Stevenson, M. Maddury

PROJECTS

2012

2012

2012

2011

Zest – Memory Deduplicator for Linux 2012 – 2016

Using LiME, zest counts duplicates in DRAM memory. Captures a snapshot of physical memory from a live instance of Linux. Performs post-mortem fine-grain deduplication to show the benefit of deduplicated memory systems. Shows that memory capacity is increased by over 2x in many common datacenter applications.

Hash-Stats

Overflow Statistics for Large Hash Tables

Table utilization and table overflows are critical issues for large hash tables, but these topics receive little attention in the literature and the CS curriculum. This repository reduces theory to practice. Using published theoretical results, it provides simple matlab scripts to guide the practicing engineer when implementing a large hash table.

https://github.com/etep/hash-stats

Stanford Circuit Optimization Tool

2008 – 2012

Using convex optimization, opimizes digital circuit design for latency and power. Integrates with industry standard tools such as SPICE.

2010 http://github.com/etep/scot

Punch Mobile

Electronic payment processing with integrated consumer loyalty. Provided significant cost savings by disintermediating the credit card payment network using a direct consumer-tobusiness (C2B) back-end. Voted as top project by VC panel.

Faculty Mentor for Solar Boat

As an officer faculty member at the U.S. Naval Academy, mentored a multidisciplinary team of undergraduates competing in the world championship of solar electric boating.

SIMD Floating Point Adder

2001

Designed and taped out a fully functional 1x32 / 2x16 bit SIMD floating point adder with IEEE compliant rounding for Stanford independent projects in VLSI, EE-271. Silicon fabricated by TSMC in 0.5 μ m technology.

2006 - 2008

2011

2016

2014